# PATMOS / VARI 2014
## SESSION OVERVIEW

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<td>8:00</td>
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<td>Registration</td>
<td>VARI Session 1</td>
<td>PATMOS Session 7</td>
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<td>Keynote: Arlindo Oliveira.</td>
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<td>CAD Techniques in</td>
<td>Variability in Memories</td>
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<td>Computational Biology</td>
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<td>Keynote: Massimo Alioto.</td>
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<td>Modeling, Simulation</td>
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<td>Power estimation</td>
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<td>Yield, Robustness and</td>
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<td>Power and Timing</td>
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19:30 Social Event and Gala Dinner
9:20 - 10:20 PATMOS Keynote 1

Title: CAD Techniques in Computational Biology

Speaker: Arlindo Oliveira

Abstract: During the last four decades, many algorithms have been developed in the area of Computer Aided Design (CAD) with the objective of supporting circuit designers in the phases of circuit design, verification and test. Coupled with the advances in VLSI technology, these algorithms are at the core of our ability to design circuits with many millions of elements. Recently, with the development of high throughput techniques for biological data and the improved knowledge of biological processes that they supported, it has been possible to design complex models for biological systems that can use many of the algorithms, formalisms and approaches that have been developed by the CAD community. Up to now, simulation and model verification techniques are the most popular tools borrowed by biologists from the CAD community. With the advent of synthetic biology, and the need for tools that support the design of complex systems, other techniques that were created by the CAD community are likely to find their place amongst the methods used by biologists and bioinformaticians in their quest for tools that help them design, simulate and validate models for new and existing biological systems.

Biography: Arlindo Oliveira got his BSc and MSc degrees from Instituto Superior Técnico (IST), in 1986 and 1989 and his PhD in 1994, from UC Berkeley, all in EECS. He has since developed research and teaching work in the areas of Circuit Design, Computer Aided Design, Algorithms, Machine Learning, Data Mining and Bioinformatics. He was a researcher at the Electronics Research Lab of UC Berkeley, of the Cadence Berkeley Laboratories and of INESC-ID, in Lisbon, Portugal, where he co-founded the Knowledge Discovery and Bioinformatics group. He is author of one book in computer architecture and of more than a hundred articles. He was director of INESC-ID (a key laboratory, in Portugal), chaired the department of Computer Science and Engineering of IST and is currently the President of IST, the largest and most prestigious engineering school in Portugal.
10:20 - 10:45 Break and Poster Session (PATMOS)

Low-Power Design Methodology for CML and ECL Circuits
Oliver Schrape. IHP, Germany
Markus Appel, Frank Winkler. Humboldt University Berlin, Germany
Milos Krstic. IHP, Germany

DOE based high performance gate-level pipelines
Juan Núñez, Héctor J. Quintero and María J. Avedillo. Instituto de Microelectrónica de Sevilla, IMSE-CNM, CSIC/Universidad de Sevilla, Spain

Power-Efficient Power-Management Logic
Dominik Macko, Katarína Jelemenská and Pavel Čičák. Slovak University of Technology in Bratislava, Slovakia

GALS Design of ECC against Side Channel Attacks - A Comparative Study
Xin Fan. IHP, Germany
Steffen Peter. University of California-Irvine, United States
Milos Krstic. IHP, Germany

VPPET: Virtual Platform Power and Energy Estimation Tool for Heterogeneous MPSoC based FPGA Platforms
Santhosh Kumar Rethinagiri, Oscar Palomar. BSC-Microsoft research center, Spain
Javier Arias. Intel-BSC Exascale Lab/ Technical University of Catalonia, Spain
Adrian Cristal, Osman Unsal. Barcelona Supercomputing Center, Spain

Low-cost Hardware Implementation of Reservoir Computers
Miquel L. Alomar, Vincent Canals, Victor Martinez-Moll and Josep L Rossello. Universitat de les Illes Balears, Spain
PATMOS / VARI 2014
Monday 29th September 2014

10:45-12:00 PATMOS Session 1: Modeling, Simulation and Circuit Optimization I

10:45 Convex Optimization of Resource Allocation in Asymmetric and Heterogeneous SoC
Amir Morad, Leonid Yavits, Ran Ginosar. Technion-Israel Institute of Technology, Israel

11:10 Equivalence of Clock Gating and Synchronization with Applicability to GALS Communication
Robert Najvirt and Andreas Steininger. Vienna University of Technology, Austria

11:35 Fast Modeling Technique for Nano Scale CMOS Inverter and Propagation Delay Estimation
Abdoul Rjoub and Areej Ahmad. Jordan University of Science and Technology, Jordan

12:00 - 13:15 PATMOS Session 2: Power Estimation

12:00 Fast and Accurate Solution for Power Estimation and DPA Countermeasure Design
Daniel Vidal and Mário Côrtes. UNICAMP, Brazil

12:25 Formal Description of an Approach for Power Consumption Estimation of Embedded Systems
Dmitriy Shorin and Armin Zimmermann. Technische Universität Ilmenau, Germany

12:50 A Methodology for Scaling Power Dissipation Values Between Different FPGAs
Axel Reimer and Wolfgang Nebel. OFFIS Institute for Information Technology, Germany
14:30 - 16:10 PATMOS Session 3: Yield, Robustness and Power Efficiency

14:30 Parametric Yield Optimization Using Leakage-Yield-Driven Floorplanning
Yang Xu, Bo Wang and Jürgen Teich. University of Erlangen-Nuremberg, Germany

14:55 Experimental Analysis of Flip-Flops Minimum Operating Voltage in 28nm FDSOI and the Impact of Back Bias and Temperature
Sébastien Bernard. CEA-LETI/UCL, France
Marc Belleville. CEA-LETI, France
Alexandre Valentian. CEA LETI / MINATEC, France
Jean-Didier Legat. UCL, Belgium
David Bol. Université catholique de Louvain, Belgium

15:20 Power Efficient Digital IC Design for a Medical Application with High Reliability Requirements
Nasim Pour Aryan. Institute for Technical Electronics, Technische Universitaet Muenchen, Germany
Nils Heidmann. Institute of Electrodynamics and Microelectronics, University of Bremen, Germany
Martin Wirnshofer. Institute for Technical Electronics. Technische Universitaet Muenchen, Germany
Nico Hellwege, Jonas Pistor, Dagmar Peters-Drolshagen. Institute of Electrodynamics and Microelectronics, University of Bremen, Germany
Georg Georgakos. Infineon Technologies AG, Germany
Steffen Paul. Institute of Electrodynamics and Microelectronics, University of Bremen, Germany
Doris Schmitt-Landsiedel. Institute for Technical Electronics, Technische Universitaet Muenchen, Germany

15:45 A Power-Efficient FPGA-Based Self-Adaptive Software Defined Radio
Chris Dobson, Kurt Rooks and Peter Athanas. Virginia Tech, United States
16:30 - 18:35 PATMOS Session 4: Power and Timing Efficiency

**16:30** Efficient dense and sparse matrix multiplication on GP-SIMD
Amir Morad, Leonid Yavits and Ran Ginosar. Technion - Israel Institute of Technology, Israel

**16:55** Impact of Computation Offloading on Efficiency of Wireless Face Recognition
Nanako Sumi, Akiya Baba and Vasily Moshnyaga. Fukuoka University, Japan

**17:20** Fast Energy Evaluation of Embedded Applications for Many-core Systems
Felipe Da Rosa. UFRGS, Brazil
Luciano Ost. LIRMM, France
Thiago Raupp, Fernando Moraes. PUCRS, Brazil
Ricardo Reis. UFRGS, Brazil

**17:45** A Global Perspective on Energy Conservation in Large Data Networks
Lisa Durbeck. Cell Matrix Corporation, United States
Peter Athanas. Virginia Tech, United States
8:30 - 10:35 VARI Session 1: Variability in Memories

8:30 Reliability Challenges in Design of Memristive Memories
Peyman Pouyan, Esteve Amat, Antonio Rubio. Polytechnic University of Catalonia (UPC), Spain

8:55 Characterization of Random Telegraph Noise and its impact on reliability of SRAM sense amplifiers
Javier Martín Martinez, Javier Diaz, Rosana Rodríguez, Montserrat Nafria, Xavier Aymerich. Universitat Autònoma de Barcelona, Spain
Elisenda Roca, Francisco Vidal Fernandez. Instituto de Microelectrónica de Sevilla, CSIC and Universidad de Sevilla, Spain
Antonio Rubio. Universitat Politècnica de Catalunya (UPC), Spain

9:20 Variability impact on on-chip memory data paths
Esteve Amat, Antonio Calomarde, Ramon Canal and Antonio Rubio. Universitat Politècnica de Catalunya (UPC), Spain

9:45 SRAM Write Margin Cell Estimation using Word-line Modulation and read/write operations
Bartomeu Alorda, Cristian Carmona, Gabriel Torrens. Universitat de les Illes Balears, Spain

10:10 Comparative Evaluation of Tunnel-FET Ultra-Low Voltage SRAMs and Impact of Variations
Massimo Alioto. National University of Singapore, Singapore
David Esseni. University of Udine, Italy
Title: Designing (Relatively) Unreliable Systems with (Highly) Unreliable Components

Speaker: Massimo Alioto

Abstract: Almost ten years after the breed of papers and keynotes speeches on the design of reliable systems with unreliable components, the design challenges posed by variations are harder than ever. To reduce the large energy cost of computational correctness due to variations, the VLSI community is now exploring ways to embrace imperfect computation, instead of over-constraining circuits/systems to hide the natural imperfection of hardware. However, the field of “approximate computing” is still in its infancy, and most of the related work is highly fragmented and not really focused on the real challenges ahead of us.

In this talk, a vision on how mainstream processing platforms can incorporate imperfect computation will be presented. In particular, we will introduce a unitary framework for systems that dynamically trade energy and “quality of computation” off, depending on the application and the user’s requirements. To address one of the key related challenges, fresh concepts to preserve the economy of scale offered by today’s design approaches will be discussed. In particular, ideas will be discussed on how to incorporate dynamic energy-quality management in general-purpose systems, designed with existing EDA tools, and programmed with existing software programming models (or so). Unsurprisingly, variation-aware and across-boundary design are two key concepts that represent a common thread for this keynote speech. To open up a broader perspective, variation-aware circuit techniques and design strategies will be discussed to enable dynamic and wide energy-quality adjustment in sub-32nm technologies, from error-tolerant to error-free. Appropriate abstractions, architectures and control schemes will be discussed to propagate such capability at all levels.

As main conclusion, imperfection and variations can actually be used to enrich the traditional perfect computational paradigm, rather than disrupt it. But this requires a
much more diffused (and profound) awareness of variations in both the hardware and the software community.

**Biography:** Massimo Alioto received the Laurea (MSc) degree in Electronics Engineering and the Ph.D. degree in Electrical Engineering from the University of Catania (Italy) in 1997 and 2001, respectively. He is an Associate Professor at the Department of Electrical and Computer Engineering, National University of Singapore. Previously, he was Associate Professor at the Department of Information Engineering of the University of Siena. He has held various positions as visiting professor at UC Berkeley, University of Michigan - Ann Arbor and EPFL, as well as visiting scientist at Intel Labs – CRL (Oregon). His interests are in energy-centric VLSI design and green integrated circuits, resiliency, near-threshold circuits, self-powered and sub-mW systems, among the others.

He has authored or co-authored more than 180 publications on journals (70) and conference proceedings, and two books. He was IEEE Distinguished Lecturer (2009-2010), and Chair of the “VLSI Systems and Applications” Technical Committee of the IEEE Circuits and Systems Society (2010-2012). He currently serves as Associate Editor in Chief of the IEEE Transactions on VLSI Systems, and served as Guest Editor of various journal special issues. He also serves or has served as Associate Editor of a number of journals (including IEEE Transactions on VLSI Systems, ACM Transactions on Design Automation of Electronic Systems, IEEE Transactions on CAS - part I, Microelectronics Journal). He was Technical Program Chair of the ICECS 2013, NEWCAS 2012 and ICM 2010 conferences, and Track Chair in several other conferences (ICCD, ISCAS, ICECS, VLSI-SoC, APCCAS, ICM).
12:00 - 13:15 PATMOS Session 5: Emerging Technologies

12:00 Evaluating the Impact of Environment and Physical Variability on the Current of 20nm FinFET Devices
Alexandra L. Zimpeck, Cristina Meinhardt, Ricardo A. L. Reis. Universidade Federal do Rio Grande, Brazil

12:25 Write Scheme for Multiple Complementary Resistive Switch (CRS) Cells
Adedotun Adeyemo, Abusaleh Jabir. Oxford Brookes University, United Kingdom
Jimson Mathew, Dhiraj Pradhan. University of Bristol, United Kingdom

12:50 A Scalable Physical Model for Nano-Electro-Mechanical Relays
Haider Alrudainy, Andrey Mokhov and Alex Yakovlev. Newcastle University, United Kingdom

14:30 - 16:10 VARI Session 2: Variability at Technology and Device Levels

14:30 Variability characterisation of nanoscale Si and InGaAs FinFETs at subthreshold
Guillermo Indalecio. CITIUS, Universidad de Santiago de Compostela, Spain
Natalia Seoane, Manuel Aldegunde, Karol Kalna. College of Engineering, Swansea University, United Kingdom
Antonio Jesus Garcia-Loureiro. CITIUS, Universidad de Santiago de Compostela, Spain

14:55 TCAD simulation of interface traps related variability in bulk decananometer MOSFETs
Vikas Velayudhan, Javier Martin, Montserrat Nafria Maqueda, Rosana Rodriguez, Marc Portí. Universitat Autònoma de Barcelona, Spain
Francisco Gamiz, Cristina Medina. University of Granada, Spain
Xavier Aymerich. Universitat Autònoma de Barcelona, Spain

15:20 Four-Injector Variability Modeling of FinFET Predictive Technology Models
Pablo Royer, Marisa Lopez-Vallejo, Fernando García Redondo, Carlos A. López Barrio. Laboratorio de Sistemas Integrados - Universidad Politécnica de Madrid, Spain

15:45 Circuit Optimization using Device Layout Motifs
Yang Xiao, Martin Trefzer. University of York, United Kingdom
Scott Roy. University of Glasgow, United Kingdom
James Walker, Simon Bale, Andy Tyrrell. University of York, United Kingdom
PATMOS / VARI 2014
Tuesday 30th September 2014

16:30-17:45 PATMOS Session 6: Modeling, Simulation and Circuit Optimization II

16:30 Gate Leakage Current Accurate Models for Nanoscale MOSFET Transistors
Abdoul Rjoub, Nedal Taradeh and Mamoun Mistarihi. Jordan University of Science and Technology, Jordan

16:55 An Analytical Model for the CMOS Inverter
Panagiotis Chaourani, Ioannis Messaris, Nikolaos Fasarakis, Maria Ntogramatzi, Sotirios Goudos and Spyridon Nikolaidis. Aristotle University of Thessaloniki, Greece

17:20 A Framework for Efficient Evaluation and Comparison of EES Models
Sara Vinco, Alessandro Sassone, Davide Lasorsa, Enrico Macii and Massimo Poncino. Politecnico di Torino, Italy

19:30 Social Event and Gala Dinner
8:30 - 10:35 PATMOS Session 7: System Level Power Management

8:30 A Lightweight-System-Level Power and Area Estimation Methodology for Application Specific Instruction Set Processors
Syed Abbas Ali Shah, Jan Wagner, Thomas Schuster and Mladen Berekovic. Chair for Chip Design for Embedded Computing TU Braunschweig, Germany

8:55 Application-aware Scaling Governor for Wearable Devices
Jae Min Kim, Minyong Kim and Sung Woo Chung. Korea University, Republic of Korea

9:20 Advanced SoC Virtual Prototyping for System-Level Power Planning And Validation
Fabian Mischkalla, Wolfgang Mueller. University of Paderborn, Germany

9:45 End-to-End Power Estimation for Heterogeneous Cellular LTE SoCs in Early Design Phases
Bo Wang, Yang Xu, Ralph Hasholzner. Intel Mobile Communications GmbH, Germany Rafael Rosales, Michael Glaß and Jürgen Teich. Friedrich-Alexander-Universität Erlangen-Nürnberg (FAU), Germany

10:10 Energy management of highly dynamic server workloads in an heterogeneous data center
Energy consumption savings in ZigBee-based WSN adjusting power transmission at application layer
Cristian Carmona, Miquel Angel Ribot and Bartomeu Alorda. Universitat de les Illes Balears, Spain

A Methodology to Evaluate Energy Saving Techniques in Data Buses Transmission
J. Sanchez, J.M. Gil-Garcia, J.A. Sainz. Electronic Technology Department . Universidad del País Vasco, Spain
Eugeni Isern and Miquel Roca. Universitat de les Illes Balears, Spain

A unique network EDA tool to create optimized ad hoc binary to residue number system converters
Giannis Petrousov and Minas Dasygenis. University of Western Macedonia, Greece

A distributed VHDL compiler and simulator accessible from the web
Minas Dasygenis. University of Western Macedonia, Greece

Optimization on Cell-library Design for Digital Application Specific Printed Electronics Circuits
Jody Matos. Federal University of Rio Grande do Sul, Brazil
Manuel Llamas, Mohammad Mashayekhi, Jordi Carrabina. Universitat Autònoma de Barcelona, Spain
André Reis. Federal University of Rio Grande do Sul, Brazil
Title: Ultra-thin Chips - a New Paradigm in Silicon Technology

Speaker: Joachim N. Burghartz

Abstract: In contrast to conventional thick silicon chips ultra-thin chips will be the basis for new applications, such as 3D integrated circuits (3D-ICs) and plastic electronics. This talk will introduce and compare two generically different process technologies that can be exploited for the fabrication of ICs on extremely thin chips. Furthermore, several application results and demonstrations will be presented and discussed based on material that has been presented at the recent IEDM and ISSCC conferences.

Biography: Joachim N. Burghartz is an IEEE Fellow, an IEEE Distinguished Lecturer, and a member of the IEEE Electron Devices Society. He received his MS degree from RWTH Aachen in 1982 and his PhD degree in 1987 from the University of Stuttgart, both in Germany. From 1987 thru 1998 he was with the IBM T. J. Watson Research Center in Yorktown Heights, New York, where he was engaged in early development of SiGe HBT technology and later in the integration of passive components, particularly inductors, for application to monolithic RF circuits. From 1998 until 2005 he was with TU Delft in the Netherlands as a full professor and from 2001 as the Scientific Director of the Delft research institute DIMES. In fall 2005 he moved to Stuttgart, Germany, to head the Institute for Microelectronics Stuttgart (IMS CHIPS). In addition he is affiliated with the University of Stuttgart as a full professor. Dr. Burghartz has published more than 250 reviewed articles and holds some 30 patents.
12:00 - 13:15 PATMOS Session 8: Low Power Techniques

12:00 Power-Efficient Turbo-Decoder Design based on Algorithm-Specific Power Domain Partitioning
Christoph Roth. ETH Zurich, Switzerland
Christian Benkeser. RUAG Space, Switzerland
Qiuting Huang. ETH Zurich, Switzerland

12:25 Design and Test of a Low-Power 90nm Xor/Xnor Gate for Cryptographic Applications
Erica Tena. IMSE-CNM/University of Seville, Spain
Javier Castro. Anafocus Company, Spain
Antonio Acosta. IMSE-CNM/University of Seville, Spain

12:50 Robust Sub-Powered Asynchronous Logic
Jiaoyan Chen. TU Delft, Netherlands
Emanuel Popovici. University College Cork, Ireland
Arnaud Tisserand. IRISA, France
Sorin Cotofana. Delft University of Technology, Netherlands

14:30 - 16:10 VARI Session 3: Variability at Circuit Level

14:30 All-digital self-adaptive PVTA variation aware clock generation system for DFS
Jordi Pérez Puigdemont, Antonio Calomarde and Francesc Moll. Universitat Politècnica de Catalunya, Spain

14:55 Adaptive Sized Quasi-Monte Carlo Based Yield Aware Analog Circuit Optimization Tool
Engin Afacan, Gönenc Berkol, Ali Emre Pusane, Günhan Dündar and Faik Başkaya. Bogazici University, Turkey

15:20 Fractional Phase Divider PLL Phase Noise and Spurious modeling
Alexandre Fonseca, Emeric De Foucauld. CEA-LETI, Grenoble, France
Philippe Lorenzini, Gilles Jacquemod. EPIB-UNS, Université Nice Sophia Antipolis, Sophia Antipolis, France

15:45 Comparison of Bulk Built-In Current Sensors in terms of Transient-Fault Detection Sensitivity
Rodrigo Possamai Bastos. TIMA Lab (CNRS - Grenoble INP - UJF), France
Jean-Max Dutertre. Ecole des Mines de Saint-Etienne, France
Frank Sill Torres. DEE, UFMG, Brazil
**16:30 - 17:45 PATMOS Session 9: Power Estimation and Optimization**

**16:30 Estimating Power Consumption of Multiple Modular Redundant Designs in SRAM-based FPGAs for High Dependable Applications**
Jimmy Tarrillo and Fernanda L. Kastensmidt. Universidade Federal do Rio Grande do Sul - UFRGS, Brazil

**16:55 Hardware-assisted Power Estimation for Design-stage Processors using FPGA Emulation**
Sebastian Hesselbarth, Tim Baumgart and Holger Blume. Leibniz Universität Hannover, Germany

**17:20 Rate-Distortion and Energy Performance of HEVC Video Encoders**
Eduarda Monteiro, Mateus Grellert. Federal University of Rio Grande do Sul, Brazil
Bruno Zatt. Federal University of Pelotas, Brazil
Sergio Bampi. Federal University of Rio Grande do Sul, Brazil

**17:45 Tuning Software-based Fault-tolerance Techniques for Power Optimization**
Eduardo Chielle, Fernanda Lima Kastensmid. Universidade Federal do Rio Grande do Sul, Brazil
Sergio Cuenca-Asensi. University of Alicante, Spain

**18:10 Closing Remarks**